AMENDMENT TO THE CLAIMS

This listing of claims will replace all prior versions of claims in the application.

Listing of Claims:

1. (currently amended) A single chip set-top box integrated circuit, comprising:

a digital BTSC encoder that is operable to encode first and second digital audio signals into a BTSC encoded signal, ~~said~~ the first and second digital audio signals having a bandwidth defined by the frequency content of ~~said~~ the first and second digital signals; ~~and~~

a digital output modulator for receiving the BTSC encoded signal and generating a radio frequency (RF) modulated output signal that is provided off chip; and

a BTSC decoder to receive a demodulated audio signal and to decode the demodulated audio signal for coupling to the digital BTSC encoder;

wherein the digital BTSC encoder, BTSC decoder and digital output modulator are integrated on a same common substrate and constructed as a single complementary metal oxide semiconductor (CMOS) integrated circuit chip and wherein data is exchanged between the digital BTSC encoder and the BTSC decoder in a digital loopback mode to co-verify the data.

2. (currently amended) The single chip set-top box integrated circuit of claim 1, wherein:

the digital BTSC encoder comprises (a) a sum channel processor comprising a first digital filter for digitally processing a digital sum signal and (b) a difference channel processor comprising a second digital filter for digitally processing a digital difference signal, wherein the digital BTSC encoder operates at a sample rate that is at least substantially ten times the bandwidth of the first and second digital audio signals so that ~~said~~ the digital filters in the sum channel processor and the difference channel processor substantially match BTSC analog filter transform functions in both magnitude and phase; and

the digital output modulator comprises an audio/video processor that is operable to encode an audio/video signal ~~thereby generating a RF modulated audio/video signal as~~ to generate the RF modulated output signal.

3. (currently amended) The single chip set-top box integrated circuit of claim 2, wherein the RF modulated ~~audio/video~~ output signal is a channel 3/4 RF modulated audio/video signal that is provided off chip ~~to at least one audio/visual playback device~~.

4. (currently amended) The single chip set-top box integrated circuit of claim 2, further comprising:

a rate converter and FM modulator, ~~communicatively~~ coupled to the audio/video processor, that modulates the BTSC encoded signal, ~~thereby generating~~ to generate a processed audio signal; and

a video processor, ~~communicatively~~ coupled to the audio/video processor, that performs video processing of a composite video signal ~~thereby generating~~ to generate a processed video signal;

wherein the audio/video processor combines the processed audio signal and the processed video signal ~~into the audio/video signal~~.

5. (original) The single chip set-top box integrated circuit of claim 1, wherein the first and second digital audio signals are Pulse Code Modulation (PCM) baseband audio source signals.

6. (currently amended) The single chip set-top box integrated circuit of claim 2, wherein the digital output modulator ~~comprises~~ includes a Digital to Analog Converter (DAC) ~~that is operable to transform a digital signal into an analog signal~~.

7. (currently amended) The single chip set-top box integrated circuit of claim 6, ~~comprising~~ further including a clock generator for generating a first clock signal for clocking the DAC and for generating a second clock signal for clocking digital logic that transfers data to the DAC.

8. (original) The single chip set-top box integrated circuit of claim 7, wherein the first and second clock signals have a phase relationship that is controlled by a phase control signal.

9. (canceled)

10. (canceled)

11. (currently amended) An integrated circuit that includes a digital audio/video system, the integrated circuit comprising:

~~(A)~~ a digital audio processor for BTSC encoding first and second digital audio signals into an encoded audio signal, ~~comprising~~ the digital audio processor including sum channel processing means and difference channel processing means;

~~(B)~~ a digital video processor that processes a composite video signal, ~~thereby generating~~ to generate a digital video signal; ~~and~~

~~(C)~~ an audio/video processor ~~that is operable~~ coupled to modulate the encoded audio signal and digital video signal to generate a Radio Frequency (RF) modulated audio/video signal that is provided off chip[,], and

a BTSC decoder to receive a demodulated audio signal and to decode the demodulated audio signal for coupling to the digital audio processor;

wherein the digital audio processor, digital video processor, ~~and~~ audio/video processor, and BTSC decoder are integrated on a same common substrate and constructed as a single complementary metal oxide semiconductor (CMOS) integrated circuit chip and wherein data is exchanged between the digital audio processor and the BTSC decoder in a digital loopback mode to co-verify the data.

12. (currently amended) The integrated circuit of claim 11, wherein the digital audio processor operates at a sample rate so that ~~said~~ sum channel processing means and the difference channel processing means substantially match BTSC analog filter transform functions in both amplitude and phase ~~whereby~~ substantially requiring no phase ~~compensation is required~~.

13. (currently amended) The integrated circuit of claim 11, wherein:

the digital audio processor is ~~communicatively~~ coupled to the audio/video processor and performs audio processing on a Pulse Code Modulation (PCM) baseband audio source signal to generate the encoded audio signal;

the digital video processor is ~~communicatively~~ coupled to the audio/video processor to generate the digital video signal; and

the audio/video processor combines the encoded audio signal and the digital video signal into the audio/video signal.

14. (currently amended) The integrated circuit of claim 11, wherein the audio/video processor ~~comprises a DAC~~ includes a Digital to Analog Converter (DAC) that is clocked with a first clock signal.

15. (currently amended) The integrated circuit of claim 14, further comprising a clock generator for generating the first clock signal and for providing a second clock signal to digital logic circuitry that transfers data to the DAC, wherein a timing relationship between the first clock signal and the second clock signal is programmably controlled.

16. (currently amended) The integrated circuit of claim 11, wherein the integrated circuit is integrated as part of a single chip set-top box ~~and further includes an IF demodulator, a video decoder, a transport processor, a high-definition MPEG video decoder, a BTSC decoder and an audio DAC as part of the single integrated circuit chip~~.

17. (canceled).

18. (currently amended) The integrated circuit of claim 11, wherein the digital audio processor operates at a sample rate that is at least approximately ten times a bandwidth of the first and second digital audio signals so that no phase compensation is required in ~~a~~ the sum channel processing means or difference channel processing means to substantially match BTSC analog filter transform functions in both magnitude and phase.

19. (currently amended) A method for modulating an audio/visual signal on a single integrated circuit chip, comprising:

receiving audio data and video data on the chip;

digitally processing the video data on the chip to generate a composite video signal;

digitally encoding the audio data on the chip using a BTSC encoder in accordance with a BTSC audio encoding standard to generate an encoded audio signal;

converting the encoded audio signal from a first sampling rate to a second sampling rate on the chip;

frequency modulating an aural carrier using the converted encoded audio signal on the chip, thereby generating a frequency modulated (FM) audio signal;

mixing the composite video signal and FM audio signal to a programmable carrier frequency on the chip, in which encoding, converting and mixing are performed in a single complementary metal oxide semiconductor (CMOS) integrated circuit chip~~, thereby generating~~ to generate an RF modulated audio/visual signal;~~and~~

outputting the RF modulated audio/visual signal off chip;

receiving an audio signal at a BTSC decoder also located in the CMOS integrated circuit chip to decode a demodulated audio signal for coupling to the BTSC encoder; and

exchanging data between the BTSC encoder and the BTSC decoder in a digital loopback mode to co-verify the data.

20. (previously presented) The method of claim 19, wherein the RF modulated audio/visual signal is a channel 3/4 RF modulated audio/video signal.

21. (currently amended) The method of claim 19, wherein~~the step of~~ when digitally encoding the audio data~~comprises~~, the encoding is performed using a sampling rate of at least approximately 150-200 kHz to generate the encoded audio signal.